S29AL008D

8-Mbit (1M x 8-Bit/512K x 16-Bit), 3 V Boot Sector Flash

This product has been retired and is not recommended for designs. For new and current designs, S29AL008J supercedes S29AL008D. This is the factory-recommended migration path. Please refer to the S29AL008J data sheet for specifications and ordering information.

Distinctive Characteristics

Architectural Advantage

- Single Power Supply Operation
  - 2.7 to 3.6 volt read and write operations for battery-powered applications
- Manufactured on 200 nm Process Technology
  - Compatible with 0.32 µm and 230 nm Am29LV800 devices
- Flexible Sector Architecture
  - One 16-Kbyte, two 8-Kbyte, one 32-Kbyte, and fifteen 64-Kbyte sectors (byte mode)
  - One 8 Kword, two 4 Kword, one 16-Kword, and fifteen 32-Kword sectors (word mode)
  - Supports full chip erase
  - Sector Protection features:
  - A hardware method of locking a sector to prevent any program or erase operations within that sector
  - Sectors can be locked in-system or via programming equipment
  - Temporary Sector Unprotect feature allows code changes in previously locked sectors
- Unlock Bypass Program Command
  - Reduces overall programming time when issuing multiple program command sequences
- Top or Bottom Boot Block Configurations Available
- Embedded Algorithms
  - Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - Embedded Program algorithm automatically writes and verifies data at specified addresses
- Compatibility with JEDEC Standards
  - Pinout and software compatible with single-power supply Flash
  - Superior inadvertent write protection

Performance Characteristics

- High Performance
  - Access times as fast as 55 ns
  - Extended temperature range (-40°C to +125°C)
- Ultra-low Power Consumption (typical values at 5 MHz)
  - 200 nA Automatic Sleep mode current
  - 200 nA standby mode current
  - 7 mA read current
  - 15 mA program/erase current
- Cycling Endurance: 1,000,000 cycles per sector typical
- Data Retention: 20 years typical
  - Reliable operation for the life of the system

Package Option

- 48-ball FBGA
- 48-pin TSOP
- 44-pin SO

Software Features

- Data# Polling and Toggle Bits
  - Provides a software method of detecting program or erase operation completion
- Erase Suspend/Erase Resume
  - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation

Hardware Features

- Ready/Busy# Pin (RY/BY#)
  - Provides a hardware method of detecting program or erase cycle completion
- Hardware Reset Pin (RESET#)
  - Hardware method to reset the device to reading array data

General Description

The S29AL008D is an 8 Mbit, 3.0 volt-only Flash memory organized as 1,048,576 bytes or 524,288 words. The device is offered in 48-ball FBGA, 44-pin SO, and 48-pin TSOP packages. For more information, refer to publication number 21536. The word-wide data (x16) appears on DQ15–DQ0; the byte-wide (x8) data appears on DQ7–DQ0. This device requires only a single, 3.0 volt V_{CC} supply to perform read, program, and erase operations. A standard EPROM programmer can also be used to program and erase the device.

This device is manufactured using Spansion's 200 nm process technology, and offers all the features and benefits of the Am29LV800B, which was manufactured using 0.32 µm process technology.

The standard device offers access times of 55, 60, 70, and 90 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device contains separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle is completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses are stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

Spansion's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

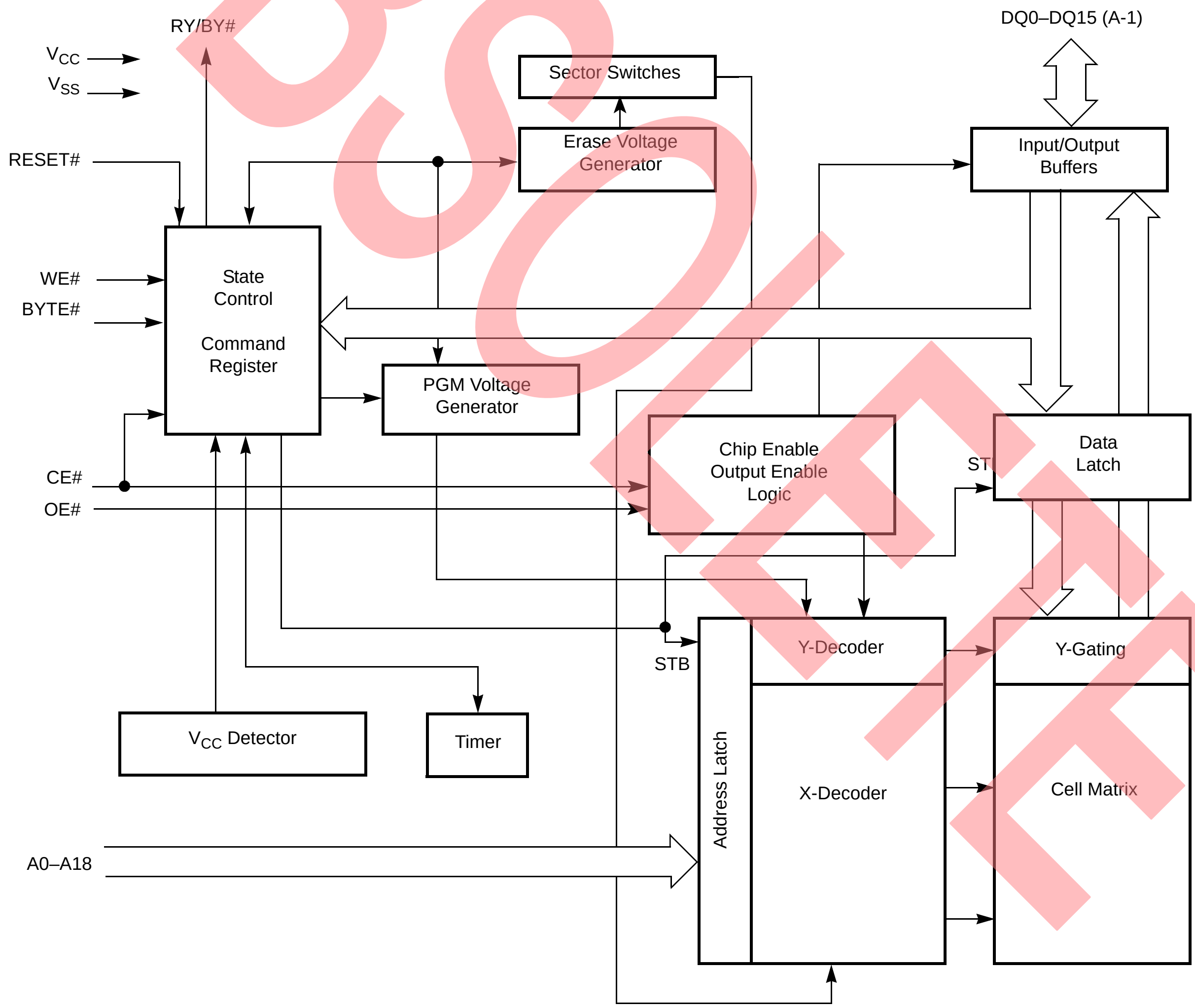
Contents

1. Product Selector Guide

Family Part Number		S29AL008D			
Speed Options	Full Voltage Range: V_{CC} = 2.7 – 3.6 V		60	70	90
	Regulated Voltage Range: V_{CC} = 3.0 – 3.6V	55			
Max access time, ns (t_{ACC})		55	60	70	90
Max CE# access time, ns (t_{CE})		55	60	70	90
Max OE# access time, ns (t_{OE})		25	25	30	35

Note
See AC Characteristics on page 30 for full specifications.

2. Block Diagram



3. Connection Diagrams

Figure 3.1 Standard TSOP

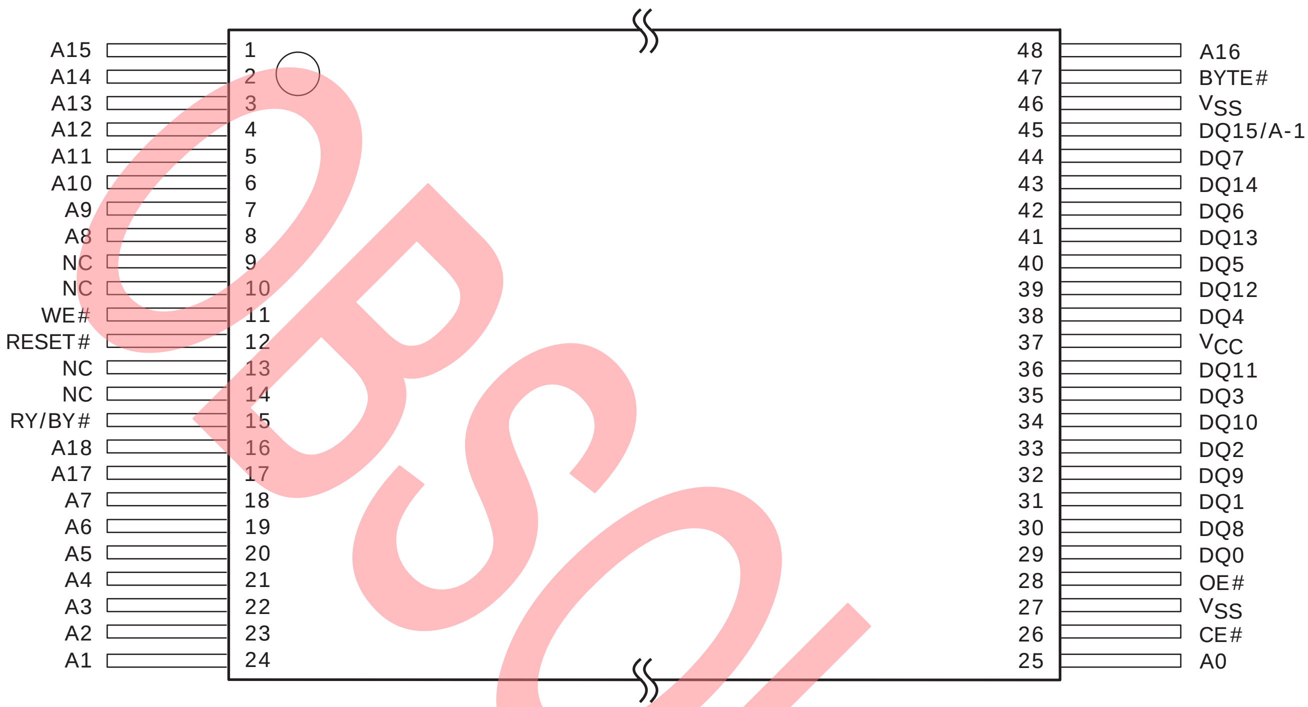


Figure 3.2 SO Pinout

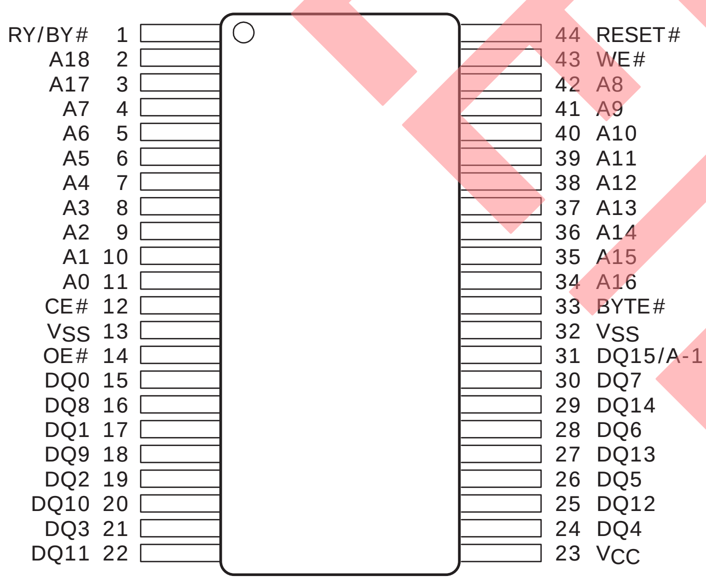
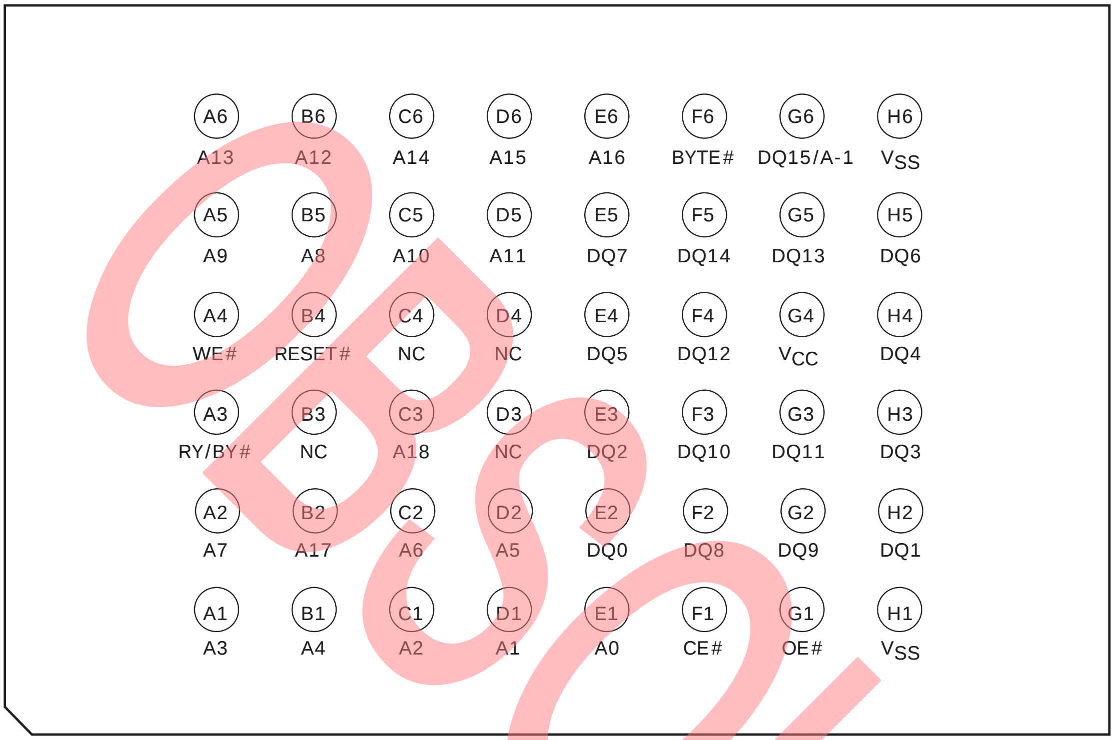


Figure 3.3 Fine-pitch BGA Pinout (Top View, Balls Facing Down)



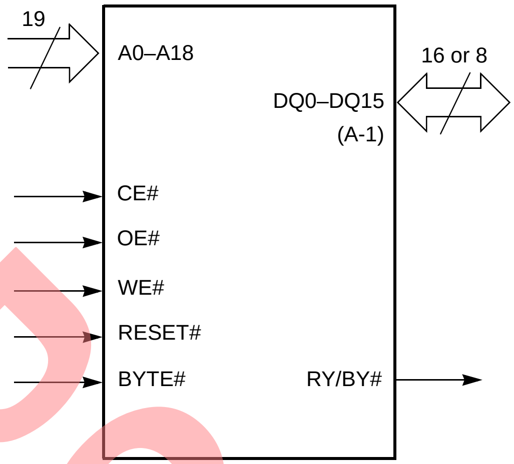
3.1 Special Handling Instructions for FBGA Package

Special handling is required for Flash Memory products in FBGA packages. Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

4. Pin Configuration

I/O Name	Description
A0–A18	19 addresses
DQ0–DQ14	15 data inputs/outputs
DQ15/A-1	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
BYTE#	Selects 8-bit or 16-bit mode
CE#	Chip enable
OE#	Output enable
WE#	Write enable
RESET#	Hardware reset pin, active low
RY/BY#	Ready/Busy# output
V_{CC}	3.0 volt-only single power supply (see *Product Selector Guide* on page 4 for speed options and voltage supply tolerances)
V_{SS}	Device ground
NC	Pin not connected internally

5. Logic Symbol

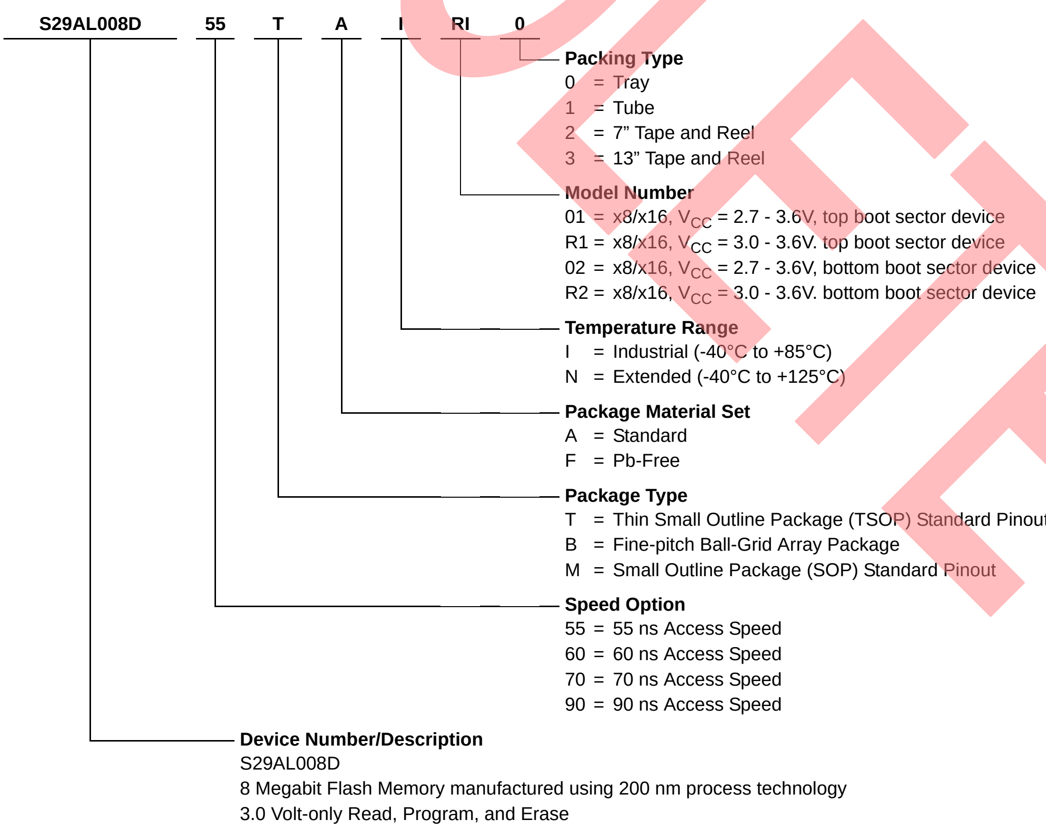


6. Ordering Information

This product has been retired and is not recommended for designs. For new and current designs, S29AL008J supercedes S29AL008D. This is the factory-recommended migration path. Please refer to the S29AL008J data sheet for specifications and ordering information.

6.1 Standard Products

Spansion standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

S29AL008D Valid Combinations					Package Description	
Device Number	**Speed Option**	**Package Type, Material, and Temperature Range**	**Model Number**	**Packing Type**		
S29AL008D	55	TAI, TFI	R1, R2	0, 3 (Note 1)	TS048 (Note 3)	TSOP
	60, 70, 90	TAI, TFI, TAN, TFN	01, 02			
	55	BAI, BFI	R1, R2	0, 2, 3 (Note 1)	VBK048 (Note 4)	Fine-Pitch BGA
	60, 70, 90	BAI, BFI, BAN, BFN	01, 02			
	55	MAI, MFI	R1, R2	0, 1, 3 (Note 2)	SO044 (Note 3)	SOP
	60, 70, 90	MAI, MFI, MAN, MFN	01, 02			

Notes
1. *Type 0 is standard. Specify other options as required.*
2. *Type 1 is standard. Specify other options as required.*
3. *TSOP and SOP package markings omit packing type designator from ordering part number.*
4. *BGA package marking omits leading S29 and packing type designator from ordering part number.*

7. Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

S29AL008D Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	Addresses (Note 1)	DQ0–DQ7	DQ8–DQ15	
							BYTE# = V_{IH}	BYTE# = V_{IL}
Read	L	L	H	H	A_{IN}	D_{OUT}	D_{OUT}	DQ8–DQ14 = High-Z, DQ15 = A-1
Write	L	H	L	H	A_{IN}	D_{IN}	D_{IN}	
Standby	V_{CC} ± 0.3 V	X	X	V_{CC} ± 0.3 V	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	X	High-Z	High-Z	High-Z
Sector Protect (Note 2)	L	H	L	V_{ID}	Sector Address, A6 = L, A1 = H, A0 = L	D_{IN}	X	X
Sector Unprotect (Note 2)	L	H	L	V_{ID}	Sector Address, A6 = H, A1 = H, A0 = L	D_{IN}	X	X
Temporary Sector Unprotect	X	X	X	V_{ID}	A_{IN}	D_{IN}	D_{IN}	High-Z

Legend
L = Logic Low = V_{IL}
H = Logic High = V_{IH}
V_{ID} = 12.0 ± 0.5 V
X = Don't Care
A_{IN} = Address In
D_{IN} = Data In
D_{OUT} = Data Out

Notes
1. *Addresses are A18:A0 in word mode (BYTE# = V_{IH}), A18:A-1 in byte mode (BYTE# = V_{IL}).*
2. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See Sector Protection/Unprotection on page 12.*

7.1 Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins DQ15–DQ0 operate in the byte or word configuration. If the BYTE# pin is set at logic *1,* the device is in word configuration, DQ15–DQ0 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic *0*, the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

7.2 Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}. The BYTE# pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See *Reading Array Data* on page 15 for more information. Refer to Table , *Read Operations* on page 30 for timing specifications and to Figure 15.1 on page 30 for the timing diagram. I_{CC1} in *DC Characteristics* on page 27 represents the active current specification for reading array data.

7.3 Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. Refer to *Word/Byte Configuration* on page 9 for more information.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The *Word/Byte Program Command Sequence* on page 16 contains details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table on page 10 and Table on page 11 indicate the address space that each sector occupies. A *sector address* consists of the address bits required to uniquely select a sector. The *Command Definitions* on page 15 contains details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the *Autoselect Mode* on page 12 and *Autoselect Command Sequence* on page 16 for more information.

I_{CC2} in *DC Characteristics* on page 27 represents the active current specification for the write mode. The *AC Characteristics* on page 30 contains timing specification tables and timing diagrams for write operations.

7.4 Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and I_{CC} read specifications apply. Refer to *Write Operation Status* on page 21 for more information, and to *AC Characteristics* on page 30 for timing diagrams.

7.5 Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{CC} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within $V_{CC} \pm 0.3$ V, the device is in the standby mode, but the standby current is greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

In *DC Characteristics* on page 27, I_{CC3} and I_{CC4} represents the standby current specification.

7.6 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC5} in *DC Characteristics* on page 27 represents the automatic sleep mode current specification.

7.7 RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device **immediately terminates** any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.3 V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS}±0.3 V, the standby current is greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a *0* (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is *1*), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to *AC Characteristics* on page 30 for RESET# parameters and to Figure 15.2 on page 31 for the timing diagram.

7.8 Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

S29AL008D Top Boot Block Sector Addresses

Sector	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal) (x8) Address Range	(x16) Address Range
SA0	0	0	0	0	X	X	X	64/32	00000h–0FFFFh	00000h–07FFFh
SA1	0	0	0	1	X	X	X	64/32	10000h–1FFFFh	08000h–0FFFFh
SA2	0	0	1	0	X	X	X	64/32	20000h–2FFFFh	10000h–17FFFh
SA3	0	0	1	1	X	X	X	64/32	30000h–3FFFFh	18000h–1FFFFh
SA4	0	1	0	0	X	X	X	64/32	40000h–4FFFFh	20000h–27FFFh
SA5	0	1	0	1	X	X	X	64/32	50000h–5FFFFh	28000h–2FFFFh
SA6	0	1	1	0	X	X	X	64/32	60000h–6FFFFh	30000h–37FFFh
SA7	0	1	1	1	X	X	X	64/32	70000h–7FFFFh	38000h–3FFFFh
SA8	1	0	0	0	X	X	X	64/32	80000h–8FFFFh	40000h–47FFFh
SA9	1	0	0	1	X	X	X	64/32	90000h–9FFFFh	48000h–4FFFFh
SA10	1	0	1	0	X	X	X	64/32	A0000h–AFFFFh	50000h–57FFFh
SA11	1	0	1	1	X	X	X	64/32	B0000h–BFFFFh	58000h–5FFFFh
SA12	1	1	0	0	X	X	X	64/32	C0000h–CFFFFh	60000h–67FFFh

S29AL008D Top Boot Block Sector Addresses

Sector	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal) (x8) Address Range	(x16) Address Range
SA13	1	1	0	1	X	X	X	64/32	D0000h–DFFFFh	68000h–6FFFFh
SA14	1	1	1	0	X	X	X	64/32	E0000h–EFFFFh	70000h–77FFFh
SA15	1	1	1	1	0	X	X	32/16	F0000h–F7FFFh	78000h–7BFFFh
SA16	1	1	1	1	1	0	0	8/4	F8000h–F9FFFh	7C000h–7CFFFh
SA17	1	1	1	1	1	0	1	8/4	FA000h–FBFFFh	7D000h–7DFFFh
SA18	1	1	1	1	1	1	X	16/8	FC000h–FFFFFh	7E000h–7FFFFh

Note

Address range is A18:A-1 in byte mode and A18:A0 in word mode. See Word/Byte Configuration on page 9.

S29AL008D Bottom Boot Block Sector Addresses

Sector	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal) (x8) Address Range	(x16) Address Range
SA0	0	0	0	0	0	0	X	16/8	00000h–03FFFh	00000h–01FFFh
SA1	0	0	0	0	0	1	0	8/4	04000h–05FFFh	02000h–02FFFh
SA2	0	0	0	0	0	1	1	8/4	06000h–07FFFh	03000h–03FFFh
SA3	0	0	0	0	1	X	X	32/16	08000h–0FFFFh	04000h–07FFFh
SA4	0	0	0	1	X	X	X	64/32	10000h–1FFFFh	08000h–0FFFFh
SA5	0	0	1	0	X	X	X	64/32	20000h–2FFFFh	10000h–17FFFh
SA6	0	0	1	1	X	X	X	64/32	30000h–3FFFFh	18000h–1FFFFh
SA7	0	1	0	0	X	X	X	64/32	40000h–4FFFFh	20000h–27FFFh
SA8	0	1	0	1	X	X	X	64/32	50000h–5FFFFh	28000h–2FFFFh
SA9	0	1	1	0	X	X	X	64/32	60000h–6FFFFh	30000h–37FFFh
SA10	0	1	1	1	X	X	X	64/32	70000h–7FFFFh	38000h–3FFFFh
SA11	1	0	0	0	X	X	X	64/32	80000h–8FFFFh	40000h–47FFFh
SA12	1	0	0	1	X	X	X	64/32	90000h–9FFFFh	48000h–4FFFFh
SA13	1	0	1	0	X	X	X	64/32	A0000h–AFFFFh	50000h–57FFFh
SA14	1	0	1	1	X	X	X	64/32	B0000h–BFFFFh	58000h–5FFFFh
SA15	1	1	0	0	X	X	X	64/32	C0000h–CFFFFh	60000h–67FFFh
SA16	1	1	0	1	X	X	X	64/32	D0000h–DFFFFh	68000h–6FFFFh
SA17	1	1	1	0	X	X	X	64/32	E0000h–EFFFFh	70000h–77FFFh
SA18	1	1	1	1	X	X	X	64/32	F0000h–FFFFFh	78000h–7FFFFh

Note

Address range is A18:A-1 in byte mode and A18:A0 in word mode. See Word/Byte Configuration on page 9.

7.9 Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Table . In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table on page 10 and Table on page 11). Table shows the remaining address bits that are don't care. When all necessary bits are set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table on page 20. This method does not require V_{ID}. See *Command Definitions* on page 15 for details on using the autoselect mode.

S29AL008D Autoselect Codes (High Voltage Method)

Description	Mode	CE#	OE#	WE#	A18 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	DQ8 to DQ15	DQ7 to DQ0
Manufacturer ID: Spansion		L	L	H	X	X	V_{ID}	X	L	X	L	L	L	X	01h
Device ID: S29AL008D (Top Boot Block)	Word	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22h	DAh
	Byte	L	L	H										X	DAh
Device ID: S29AL008D (Bottom Boot Block)	Word	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22h	5Bh
	Byte	L	L	H										X	5Bh
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	L	H	L	X	01h (protected)
														X	00h (unprotected)

Legend
L = Logic Low = V_{IL}
H = Logic High = V_{IH}
SA = Sector Address
X = Don't care.

7.10 Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

The device is shipped with all sectors unprotected. Spansion offers the option of programming and protecting sectors at its factory prior to shipping the device through Spansion's ExpressFlash™ Service. Contact an Spansion representative for details.

It is possible to determine whether a sector is protected or unprotected. See *Autoselect Mode* on page 12 for details.

Sector Protection/unprotection can be implemented via two methods.

The primary method requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 7.2 on page 14 shows the algorithms and Figure 15.12 on page 37 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle.

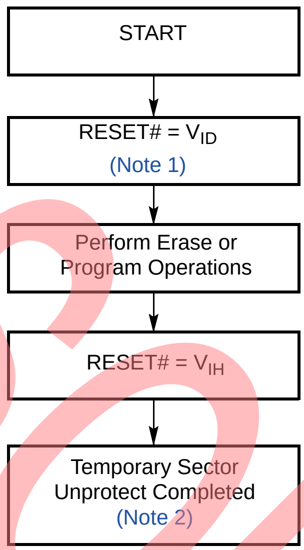
The alternate method intended only for programming equipment requires V_{ID} on address pin A9 and OE#. This method is compatible with programmer routines written for earlier 3.0 volt-only Spansion flash devices. Publication number 20536 contains further details; contact an Spansion representative to request a copy.

7.11 Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again.

Figure 7.1 shows the algorithm, and Figure 15.11 on page 37 shows the timing diagrams, for this feature.

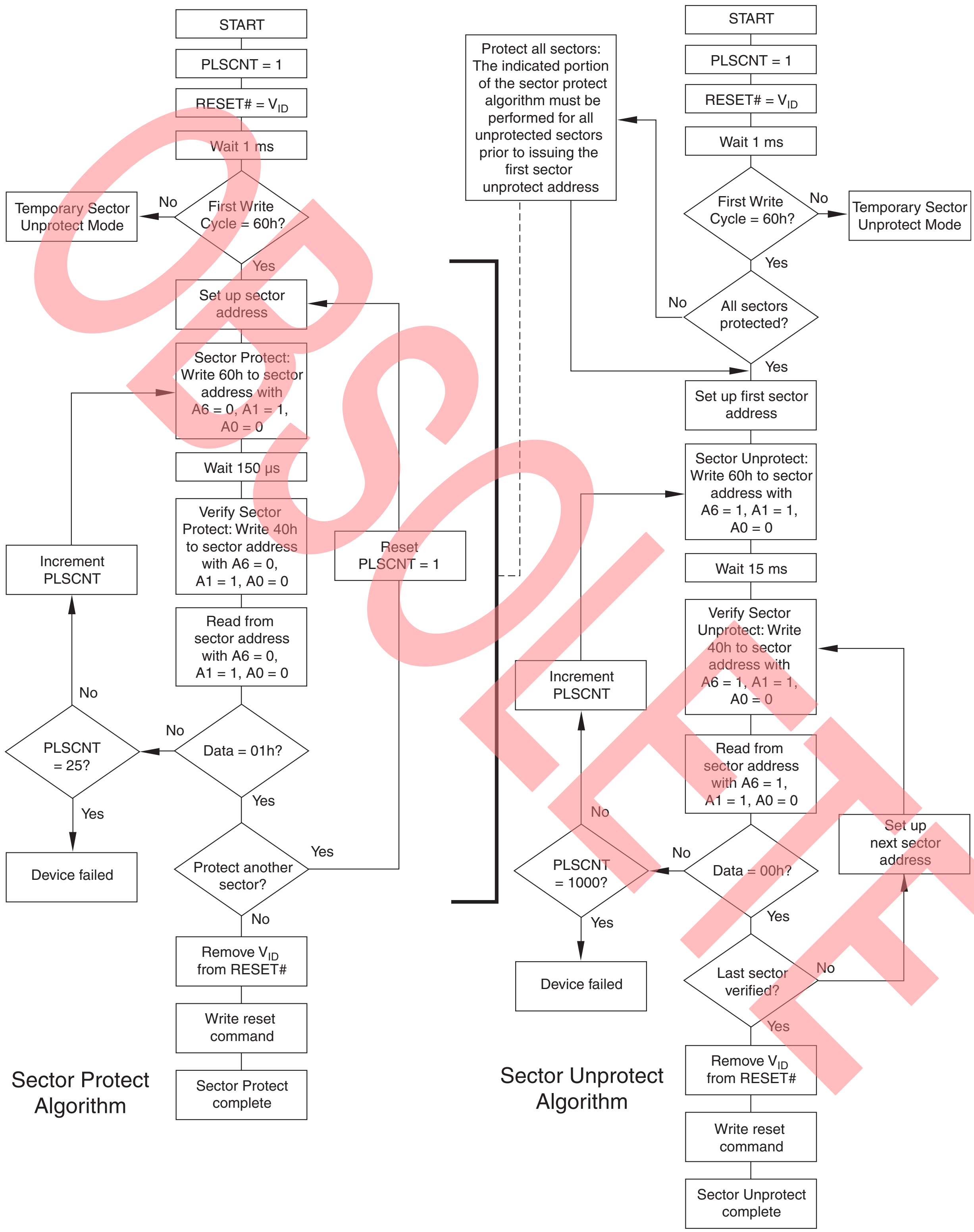
Figure 7.1 Temporary Sector Unprotect Operation



Notes

1. *All protected sectors unprotected.*
2. *All previously protected sectors are protected once again.*

Figure 7.2 In-System Sector Protect/Sector Unprotect Algorithms



7.12 Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table on page 20 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

7.12.1 Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

7.12.2 Write Pulse *Glitch* Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

7.12.3 Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

7.12.4 Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.

8. Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table on page 20 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the appropriate timing diagrams in the *AC Characteristics* on page 30.

8.1 Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See *Erase Suspend/Erase Resume Commands* on page 19 for more information on this mode.

The system *must* issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See *Reset Command* on page 16.

See also *Requirements for Reading Array Data* on page 9 for more information. Table , *Read Operations* on page 30 provides the read parameters, and Figure 15.1 on page 30 shows the timing diagram.

8.2 Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command *must* be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

8.3 Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. Table on page 20 shows the address and data requirements. This method is an alternative to that shown in Table on page 12, which is intended for PROM programmers and requires V_{ID} on address bit A9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence.

A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address XX01h in word mode (or 02h in byte mode) returns the device code. A read cycle containing a sector address (SA) and the address 02h in word mode (or 04h in byte mode) returns 01h if that sector is protected, or 00h if it is unprotected. Refer to Table on page 10 and Table on page 11 for valid sector addresses.

The system must write the reset command to exit the autoselect mode and return to reading array data.

8.4 Word/Byte Program Command Sequence

The system may program the device by word or byte, depending on the state of the BYTE# pin. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table on page 20 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. See *Write Operation Status* on page 21 for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the programming operation. The program command sequence should be reinitiated once the device resets to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a *0* back to a *1*.** Attempting to do so may halt the operation and set DQ5 to *1*, or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read shows that the data is still *0*. Only erase operations can convert a *0* to a *1.*

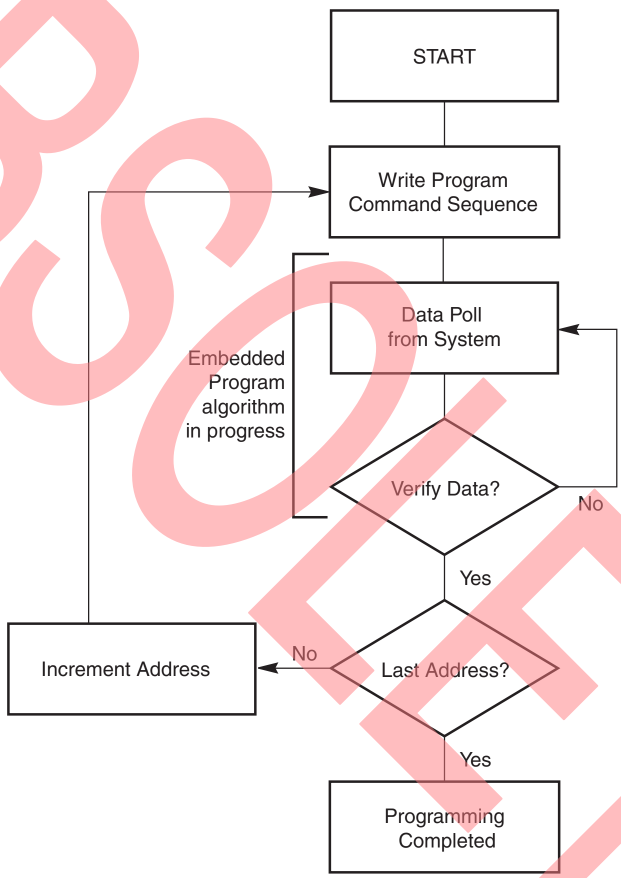
8.5 Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes or words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are don't care for both cycles. The device then returns to reading array data.

Table 8.1 illustrates the algorithm for the program operation. See *Erase/Program Operations* on page 33 for parameters, and Figure 15.5 on page 33 for timing diagrams.

Figure 8.1 Program Operation



Note
See Table on page 20 for program command sequence.

8.6 Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table on page 20 shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. Note that a **hardware reset** during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the device returns to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. See *Write Operation Status* on page 21 for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 8.2 on page 19 illustrates the algorithm for the erase operation. See *Erase/Program Operations* on page 33 for parameters, and Figure 15.6 on page 34 for timing diagrams.

8.7 Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. Table on page 20 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 µs, the system need not monitor DQ3. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data.** The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. (See *DQ3: Sector Erase Timer* on page 24.) The time-out begins from the rising edge of the final WE# pulse in the command sequence.

Once the sector erase operation begins, only the Erase Suspend command is valid. All other commands are ignored. Note that a **hardware reset** during the sector erase operation immediately terminates the operation. The Sector Erase command sequence should be reinitiated once the device returns to reading array data, to ensure data integrity.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. Refer to *Write Operation Status* on page 21 for information on these status bits.

Figure 8.2 on page 19 illustrates the algorithm for the erase operation. Refer to *Erase/Program Operations* on page 33 for parameters, and to Figure 15.6 on page 34 for timing diagrams.